The Development of a Real-Time Integration Processing Technique for PCM data between Asynchronous Master and Slave Telemetry

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ABSTRACT

In this paper, we describe the development of a real-time integration processing technique for PCM data between asynchronous master and slave Telemetry. In a synchronization parallel processing method of a real-time integration processing technique, the slave encoder receives a DSSP(Dual Sync Start Pulse) as a reference start pulse from master encoder and synchronizes the clock by generating the clock synchronized with master encoder to overcome the limitation of synchronization processing time between asynchronous master and slave Telemetry. The slave encoder transmits processed PCM data according to synchronization clock of slave encoder to master encoder. The master encoder outputs integrated PCM data in real time. After implementing the synchronization parallel processing method, we prove that the designed logic operates normally using signal tap. Also, we verify that data real-time integration processing is possible within one frame cycle through processing time test.

INTRODUCTION

Telemetry measures analog, discrete, and digital signals on various platforms and transmits wirelessly them to ground station. The received data is used to monitor the state of aircraft. Recently, Telemetry video integration device transmitting efficiently by integrating Telemetry data and video data is developed[1][2]. Lately, Telemetry requires high volume processing, rise of measurable sensor, and fast processing speed. At the same time, as the aircraft shape becomes more complex, space arrangement and size of Telemetry is limited. The size-limited Telemetry is not able to accommodate all sensors required for measurement. Also, wiring is difficult as the number and length of cable are increased to reach dispersed sensors.

To solve these problems, we developed a real-time integration processing technique for PCM data between asynchronous master and slave Telemetry in this paper. The real-time integration processing technique for PCM data between asynchronous master and slave Telemetry increases the number of measurable sensors by adding the Telemetry. The master Telemetry integrates the PCM data generated from master and slave Telemetry(hereinafter master, slave) using this technique and transmits to ground station. In the synchronization parallel processing method developed for clock synchronization between master and slave, slave receives reference pulse DSSP from master and generates synchronization clock. Finally, slaver transmits synchronized data to master. Because the slave transmits synchronized data to master, the master can reduce SYNC processing time and integrate it within one frame cycle. This paper is organized as

follows. Section 1 describes the outline of Telemetry and proposed concept. Section 2 describes the synchronization parallel processing method. Section 3 describes the verified results by using Signal Tap about implemented technique. Finally, the conclusions are given.

1. The outline of Telemetry development

1.1 The outline of Telemetry

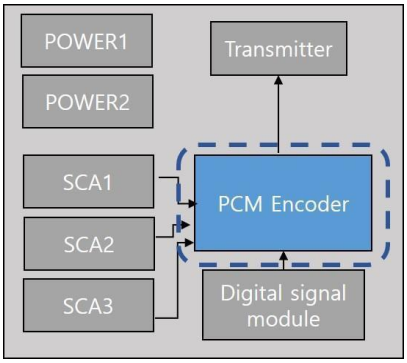

Figure 1 The block diagram of Telemetry

Figure 1 is the block diagram of Telemetry. Telemetry consists of seven modules and a transmitter. The power modules are Power module #1 and Power module #2. The Signal Conditioning Amplifier(SCA) consists of three modules(SCA1, SCA2, SCA3 respectively). The processing module of digital signal follows RS422 communication protocol. The PCM encoder module generates PCM NRZ(Non Return to Zero) frame by integrating analog, discrete, and RS422 digital signals.

1.2 The limitation of existing Telemetry and proposed concept

Although the number of sensors required for measurement is rising, the space arrangement of Telemetry is limited due to limitation of aircraft space. The existing size-limited Telemetry is not able to accommodate all sensors required for measurement. Also, wiring is difficult as the number and length of cable are increased to reach dispersed sensors. There is a method adding the PCM encoder in surplus space of aircraft for adding the number of dispersed sensors. This method is effective for reducing the required amount of cables required to reach sensors. However, when each Telemetry transmits wirelessly the PCM data to ground station, the cost is expected to increase accordingly. Therefore, we propose a method for wireless transmission from single Telemetry by integrating the PCM data of each Telemetry PCM encoder into one frame. We defined the Telemetry responsible for integrating PCM data and wireless transmission as master and the other Telemetry as slave.
Figure 2 is the block diagram of master and slave. The slave does not handle digital signal data unlike the master for space efficiency. The slave transmits a frame outputted by the slave's PCM encoder to the master. Then, the master transmits wirelessly a integrated frame to ground station.

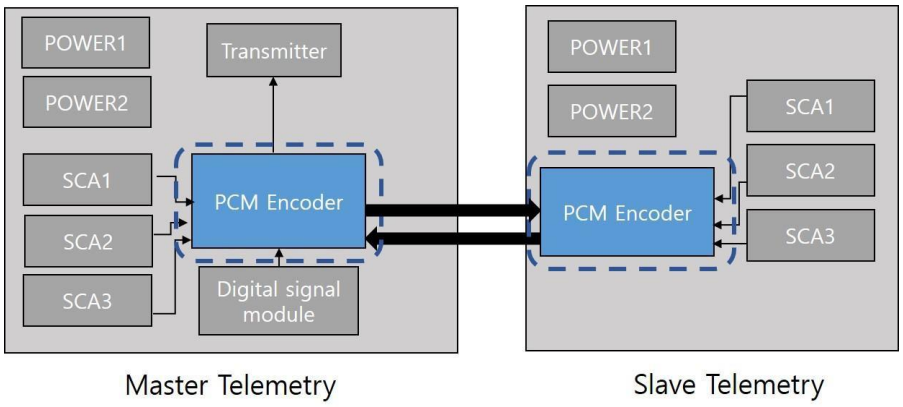

Figure 2 The block diagram of master and slave Telemetry

The PCM encoder module generates a frame in the form of PCM NRZ-L code level by measuring analog, discrete, and digital signal. The PCM encoder module of master integrates frames received from slave. A core method for integrating PCM data between PCM encoders of master and slave is the synchronization between PCM encoders and the method for encoder selection by channel. The synchronization between PCM encoders is required to clock synchronization, bit control counter, and the initialization point synchronization of channel control counter. The bit control counter and channel control counter are own variables for composition of a channel and a frame. The bit control counter is a variable that counts from 0 to 9 because a channel consists of 10-bits. The channel control counter is a variable that counts from 0 to N-1 because a frame consists of N channels. If the control counter between master and slave does not match, the correct integration cannot be achieved. The synchronization in communication is to match and maintain the temporal relationship for sending and receiving data between transmission side and reception side. There are three types of synchronization methods: external reference synchronization, inter-synchronization, and dependent synchronization. The external reference synchronization method provides the reference synchronization clock to each device simultaneously from the outside. The inter-synchronization method has multiple reference clocks and selects the best clock through inter-device cooperation. The dependent synchronization method uses the stable clock of the central device as the master clock, and the subordinate device restores the clock with clock information and uses it as its own clock[4]. We used the dependent synchronization method for achieving real-time processing performance in restricted space. The direct communication method for the clock synchronization between master and slave is not considered because it is vulnerable to cable length between master and slave. Figure 3 is a conceptual diagram related selection method of encoder by channel. The selection method of encoder by channel composes an integrated frame by referring to a Lookup Table. The Lookup Table records whether to choose master or slave for each channel. The Lookup Table can be varied to meet the needs of the user. In the Lookup Table, the master is set to 0 and the slave is set to 1 in advance. The selection method of encoder by channel composes an integrated frame by using a preset Lookup Table by determining whether the valid data on each channel is master or slave in real time. Finally, the outputted integration frame consists of the same number of channels as each frame of the master and slave.

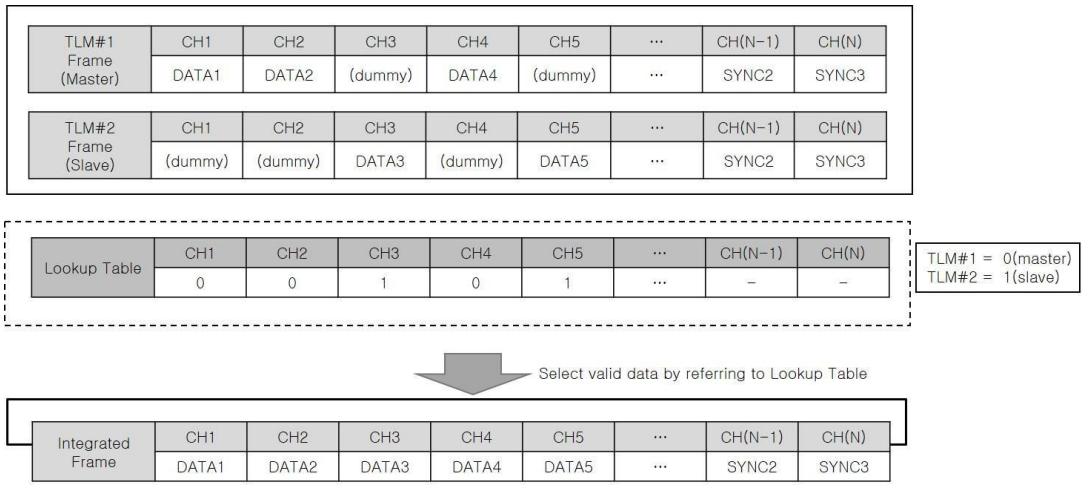

Figure 3 The conceptual diagram of encoder selection method

2. The synchronization parallel processing method

2.1 The basic concept

2.1.1 A reference start pulse for parallel processing

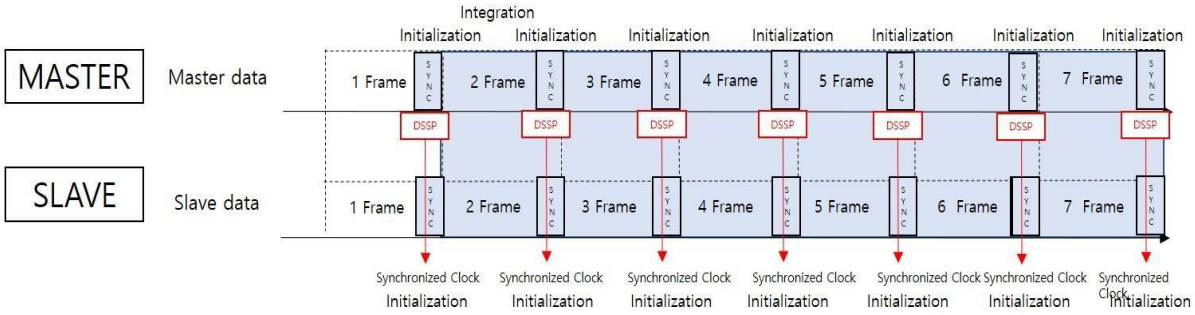

Figure 4 The conceptual diagram of synchronization parallel processing method

The synchronization parallel processing method uses a DSSP as reference start pulse. The master encoder generates a DSSP and transmits it to the slave encoder. Then, the slave encoder receives a DSSP and synchronizes the clock. Also, the slave encoder initializes the bit control counter and the channel control counter at the same time as the master encoder. The master encoder transmits a DSSP to slave encoder in every frame cycle. After receiving the DSSP, the slave encoder is initialized. The slave encoder eliminates cumulative errors caused by an oscillator through this procedure. The time point when a DSSP is transmitted by the master encoder was designed as the time point when SYNC information was retrieved and outputted from the ROM table. In this time point, the master encoder does not measure and receive analog, discrete, and digital signal. Therefore, even if clock phase is changed, there is no problem in configuring the integrated PCM frame. Figure 4 shows the process of sending and receiving a DSSP of master and slave encoder over time. It can be seen that the clock is synchronized by using a DSSP for each frame.

2.1.2 Data processing flow

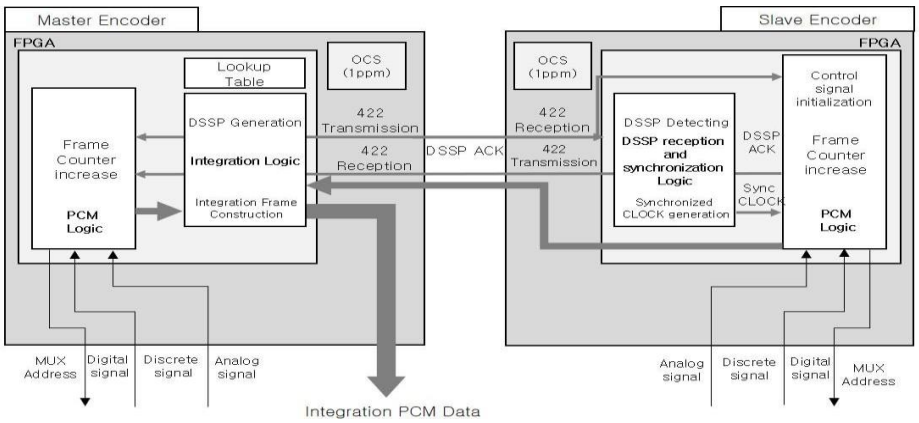

Figure 5 The data flow of synchronization parallel processing

Figure 5 is a block diagram of data processing flow for the synchronization parallel processing method. The integration logic of master encoder generates a DSSP and transmits it to slave through the 422 line. The PCM logic of the master encoder initializes a bit control counter and a channel control counter. After the slave encoder receives a DSSP, it generates a synchronized clock with the master encoder in DSSP reception and synchronization logic. The PCM logic of the slave encoder initializes a bit control counter and a channel control counter using generated clock to synchronize between encoders of the master and the slave in real time. The PCM logic of the slave encoder generates an acknowledge(ACK) as a DSSP reception response signal and transmits it to the master encoder. The master encoder receives a DSSP ACK and initializes the frame counter. In the normal state, a DSSP ACK remains high, so the frame counter is initialized only once until communication is cut off. During the above process, the PCM logic of master and slave encoder collect each channel signal through MUX address control. The PCM logic of master and slave encoder constructs collected channel signals into frames using a control counter and transmits to the integration logic of master encoder. The integration logic of master encoder receives the PCM data from PCM logic of master and slave encoder. It integrates and outputs data in real time by referring to the Lookup Table.

2.1.3 Method logic

2.1.3.1 Logic flow

Figure 6 presents the logic flow of master and slave encoder and N-channel integration structures. The PCM logic of master and slave encoder generates a frame composed of N channels respectively and transmits them to an integration logic of master encoder. The integration logic of master encoder integrates each frame into one N-channel frame by referring to the Lookup Table.

2.1.3.1.1 Master encoder logic

The integration logic of master encoder generates a DSSP signal in every frame cycle and transmits it to slave encoder through 422 line. At the same time, it initializes bit control counter

and channel control counter. When the master encoder receives a DSSP ACK signal from slave encoder, it initializes a frame counter to match a frame counter of master encoder and slave encoder. Because a DSSP ACK remains high in the normal state, the initialization of the frame counter occurs only once.

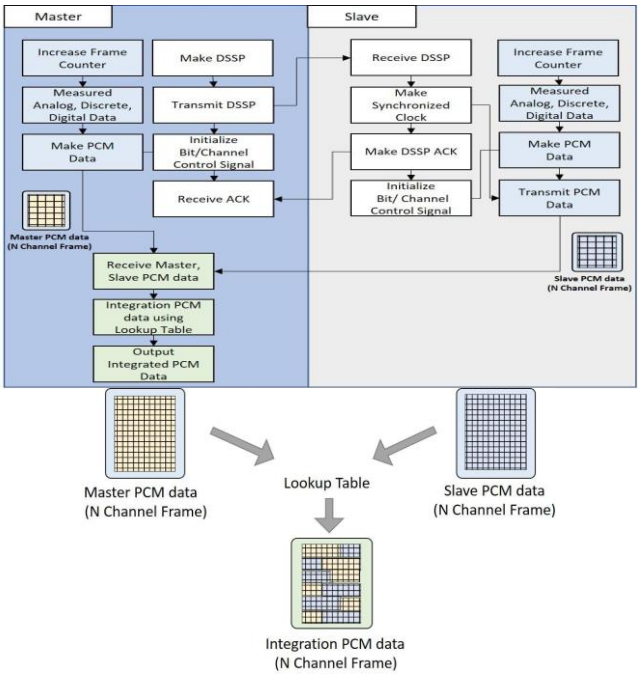

Figure 6 The logic flow of master and slave encoder and channel integration

The PCM logic of master encoder receives analog, discrete, and digital data from other modules, simultaneously increases the frame counter and constructs PCM data of master encoder. The PCM logic of master encoder sends PCM data of master encoder to the integration logic of master encoder. The integration logic of master encoder receives PCM data of slave encoder through 422 line. The integration logic of master encoder saves PCM data of master and slave encoder in 10-bit unit buffer. Then, the integration logic of master encoder constructs integrated frame by referring to the Lookup Table and outputs it.

2.1.3.1.2 Slave encoder logic

The DSSP reception and synchronization logic of slave encoder receives a DSSP from the integration logic of master encoder in every frame cycle. It generates a synchronized clock with the integration logic of master encoder. The PCM logic of the slave encoder generates an acknowledge(ACK) and transmits it to the master encoder. When a DSSP ACK is occurred to match the frame counter with the PCM logic of the master encoder, the PCM logic of the slave encoder initializes the frame counter. Because a DSSP ACK remains high in the normal state, the initialization of the frame counter occurs only once. The PCM logic of the slave encoder initializes a bit control counter and a channel control counter to synchronize PCM data with master encoder. The PCM logic of slave encoder measures analog, discrete signal and simultaneously increases the frame counter and constructs PCM data of slave encoder. After the

clock is synchronized, the PCM logic of slave encoder transmits PCM data of slave encoder to the integration logic of master encoder in real time.

3. Experiment and consideration

3.1 Hardware Implementation

Master Encoder	Slave Encoder
	

Table 1 The encoder module picture

Table 1. is a picture of the implemented encoder hardware and presents the front of master and slave encoder modules.

Item	Content
Communication Method	RS422
422 Transceiver	MAX13086EASD+
PCM data transmission speed	1.024Mbps

Table 2 Encoder communication specification

The communication specifications between master and slave encoder are shown in Table 2. Each operation logic of the master and slave is implemented by using Altera CycloneⅢ FPGA EP3C25E144 in QuqrtusⅡ 12.1 environment. Both master and slave encoder were implemented in VHDL(VHSIC Hardware Description Language) without using the C language to avoid falling into the idle state. As other parts, we use a precise oscillator with error of 1ppm, a MAX13086EASD for 422 communication, a MAX1876MIA for 12 Bit A/D Converter, a PGA206 for controlling the Gain, a regulator for supplying power.

3.2 The verification of the integration processing using the Signal Tap

3.2.1 The concept of the integration processing

The integration processing uses a Lookup Table. The integration processing of channel unit is as follows. The integration logic of master encoder receives the PCM data of master and slave encoder according to the clock of 1.024MHz. The integration logic of master encoder saves the PCM data of master encoder in the 10-bit master buffer and saves the PCM data of slave encoder in the 10-bit slave buffer by shifting from LBS(Least Significant Bit). The integration logic of master encoder saves 10-bit data in a buffer and simultaneously reads the Lookup Table to set whether significant measurement data currently being received is data from a master encoder or data from a slave encoder. The integration logic of master encoder saves the valid data in shift buffer in every 10-bit cycle. Then, it outputs finally the integrated PCM data by shifting from

MSB(Most Significant Bit). Figure 7 is a conceptual diagram constructing a frame by repeating integration processing in channel unit. The integration logic of master encoder selects the master channel or slave channel by referring to the Lookup Table and constructs a frame by setting the clock of 1.024MHz.

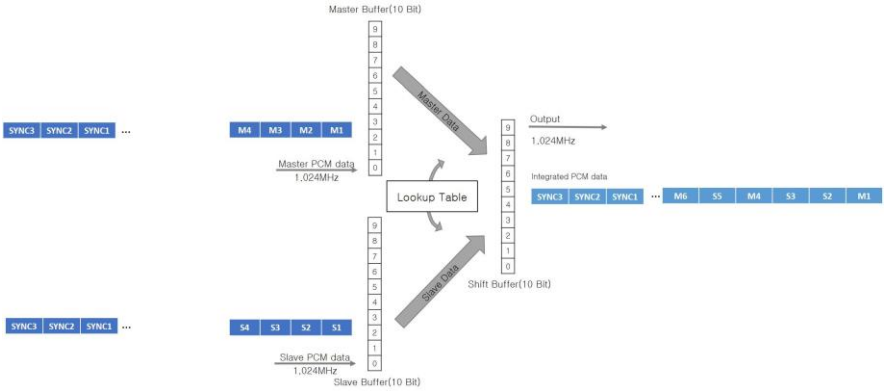

Figure 7 The conceptual diagram of integration processing

The integration logic of master encoder can know the number of the currently outputted channel using the channel control counter. The final three channel of a frame consists of SYNC.

3.2.2 The output verification of integrated data

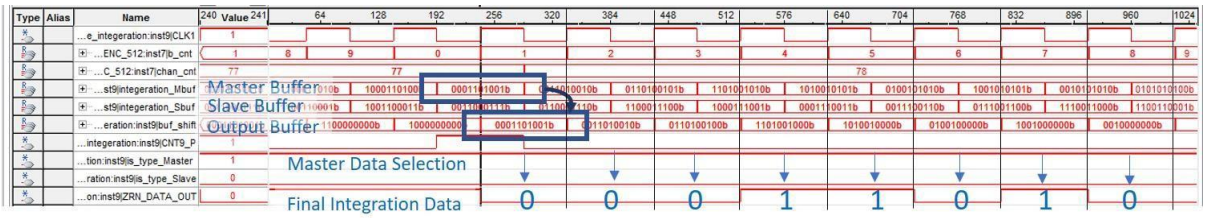

Figure 8 The selection of master data

Figure 8 and Figure 9 show the buffer items of master and slave using a Signal Tap. The PCM data of master encoder and slave encoder are received according to the clock of 1.024MHz. You can see that it is saved in each 10-bit buffer. At this time, since it is saved from the LSB, the bits of the buffer are in reverse order of the existing data bits. At the same time that 10-bit data is saved in the master and slave buffers, the type master and type slave are set by referring to the Lookup Table to determine whether the valid channel is PCM data of master or PCM data of slave. Thereafter, the valid data determined by the Type Signal among the data saved in each buffer is saved in the output buffer at 10-bit cycle, this data is shifted from MSB and outputs as final integrated PCM data. Figure 8 shows the case of selecting master data by Type Signal. The "0001101001" saved in output buffer is outputted as final integrated data by one bit from MSB. After the buffer data of master and slave is saved in output buffer, each buffer repeats the process of determining valid data at 10-bit cycle while saving the next data. In this way, the PCM data of master and slave is integrated in real time.

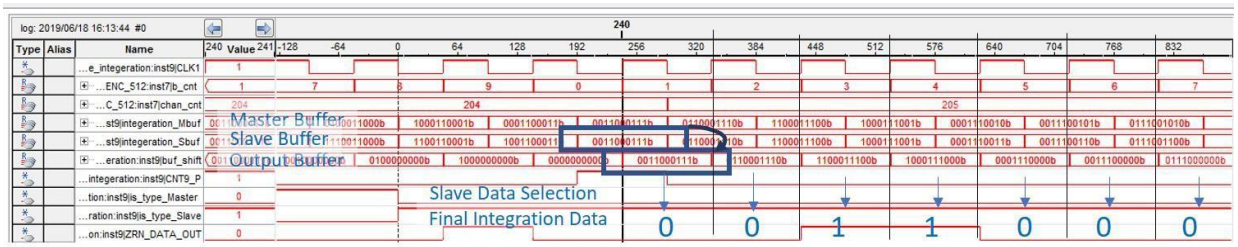

Figure 9 The selection of slave data

Figure 9 shows the case of selecting slave data by Type Signal. The "0011000111" saved in output buffer is outputted as final integrated data by one bit from MSB.

3.3 Processing time experiment

3.3.1 Experimental configuration

The experiment is carried out by mounting PCM encoder of master and PCM encoder of slave on a Telemetry. The experimental procedure is as follows. Place each Telemetry at room temperature and connect the connecting cable. Connect each Telemetry to one power supply and apply power at the same time. The frame counter and the own signal of Telemetry were saved through inspection equipment so that it could be checked with the inspection program. We repeatedly performed the experiment and confirmed that the same results were obtained.

3.3.2 Experimental Results and Considerations

Table 3 shows the experimental results of processing time for synchronization parallel processing method. It presents the frame counter and the self-signal of 20V of master and slave. When the master and slave are powered, the master can be seen outputting a data frame integrated with slave after one frame point. The parallel processing method uses the pulse signal generated in the logic as the criterion for synchronization regardless of the internal content of the frame. Therefore, slave sends synchronized data to master in real time because master does not need a process to check the SYNC. As a result, the synchronization parallel processing method enables data integration processing in real time within one frame cycle.

Time(s)	Communication Error (1:error, 0:normal)	Master Frame Count	Master_ 20V_ EXT	Slave Frame Count	Slave_ 20V_ EXT	Note
-tx4	1	1023	49.90	1023	49.90	
-tx3	1	1023	49.90	1023	49.90	
-tx2	1	1023	49.90	1023	49.90	
-t	1	1023	49.90	1023	49.90	
0	1	1023	49.90	992	-50	Power ON
t	0	2	20.01	2	19.62	Integration Data
tx2	0	3	20.01	3	19.62	
tx3	0	4	20.01	4	19.72	
tx4	0	5	20.01	5	19.72	
tx5	0	6	20.01	6	19.72	
tx6	0	7	20.01	7	19.72	
tx7	0	8	20.01	8	19.72	
tx8	0	9	20.01	9	19.72	

Table 3 The experimental results of processing time for synchronization parallel processing method

CONCLUSIONS

In this paper, we describe a technique constructing a PCM data frame by integrating data of the master encoder and slave encoder in real time for expanding the encoder function of existing Telemetry. The data integration technique has the effect of overcoming the limitation of the number of sensor measurement signals due to the spatial constraint of the aircraft, reducing the cable requirements required for physically distributed sensor access and simplifying wiring. In order to overcome the limitation of synchronization processing time in synchronization parallel processing method, the slave processes data according to the synchronization clock and transmits it to the master. This method uses a DSSP as a reference signal generated in every frame period by master. After the slave receives a DSSP, it restores a clock and initializes each control counter and sends generated PCM data to the master. The synchronized PCM data of master and slave is selected for each channel by referring to the Lookup Table and outputs the final integrated PCM data. After implementation, the designed logic is verified to operate normally by using the Signal Tap. Also, through the processing time experiments, it is verified that the integration processing method can integrate data within one frame. As a result, we demonstrate that this technique can achieve real-time integration processing performance, measure large amount of sensor data in space efficient way, and obtain high-quality Telemetry data normally.

Acknowledgements

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